AM8275
4K UHD MULTIMEDIA SOC

DATASHEET

! "#$%&$' %
(' (')'&)(' %
%
%

; 0NI " %G0% 4 GH1 " H12%

&$ 9 "H" L0I% / "2PLFQ1FGH% $$$$$$$$ %-
($ R" 01JL" 2$ $$$$$$$$ %,
S$ TIGPU% / F0VL0K$ $$$$$$$$ & '
W$ =FP "H2" 2% $$$$$$$$ &&
.$ 6FH% * 22FVHK "H12% $$$$$$$$ &(

X$ 6FH% / "2PLFQ1FGH2$ $$$$$$$$ &S
-$ <M21" K% 9 IGN0I% ! "2GJLP" 2$ $$$$$$$$ %(-

,$ / / ! % 4 GH1LGII "L% @HF1% $$$$$$$$ S(

Y$ RI023% 4 GH1LGII "L% $$$$$$$$ SX

&'$ " + + 4% 4 GH1LGII "L$ $$$$$$$$ S,

&&$ 9 "H" L0I% < 6 8% 8H1 "L00P" % $$$$$$$$ SY

&$ 9 "H"LOI% / "2PLFQ1FGH%

($ R"01JL"2%

S$ TIGPU%

. $ 6FH%*22FVHK"H12%

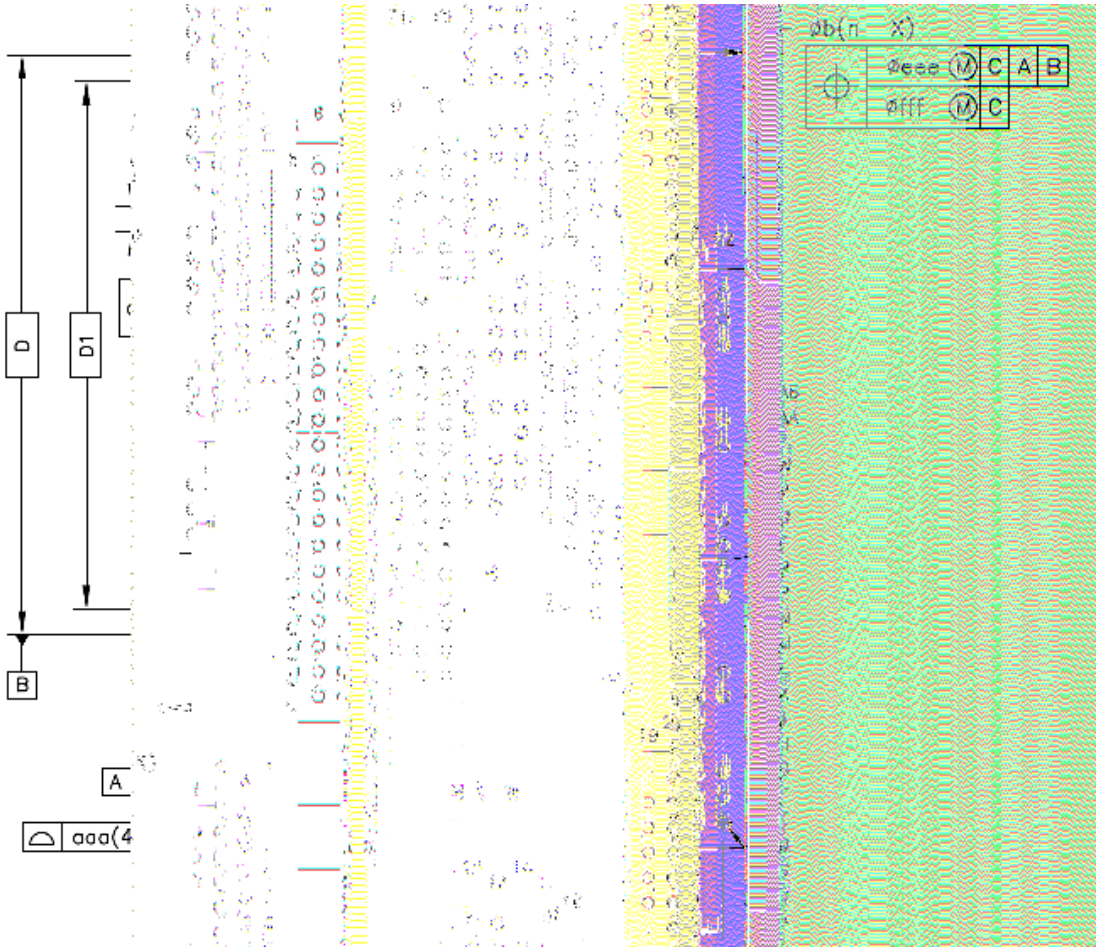


Figure 2. Pin Assignments (Bottom View)

6FH%AG$%	6FH%A0K"%	8)5%	/"0JI1%E0IJ"%	/"2PLFQ1FGH%

6FH%AG$%	6FH%A0K"%	8) 5 %	/ "0JI1%E0IJ"%	/ "2PLFQ1FGH%

6FH%AG$%	6FH%A0K"%	8)5%	/"0JI1%E0IJ"%	/"2PLFQ1FGH%

6FH%AG$%	6FH%A0K"%	8) 5 %	/ "0JI1%E0IJ"%	/ "2PLFQ1FGH%

6FH%AG$%	6FH%A0K"%	8)5%	/"0JI1%E0IJ"%	/"2PLFQ1FGH%

6FH%AG$%

6FH%AG$%	6FH%A0K"%	8)5%	/"0JI1%E0IJ"%	/"2PLFQ1FGH%

6FH%AG$%	6FH%A0K"%	8)5%	/"0JI1%E0IJ"%	/"2PLFQ1FGH%

-$ <M21"K%9IGN0I%!"2GJLP"2%

Table 2. Power Supply Specification

Table 4. DC Characteristics

<MKNGI%		+ FH$%	; MQ$%	+ 0 \ $%	@HF1%	/ "2PLFQ1FGH%

Table 6. Crystal Requirements for the AM8275

<MKNGI%	/ "2PLFQ1FGH) 4 GH [F1FGH%	+ FHFKJK%	; MQFP0I%	5 00 T4 23 5

Figure

Table 10. Power-On Reset Trigger Level

,$ / / ! %4GH1LGII"L%@HF1%

!

6FH%A0K"%	;MQ"%	/ "2PLFQ1FGH%

Table 12. DCU Block External Pin Mux Table

T0II%AJKN"L%	/ / ! S%	/ / ! W%

T0II%AJKN"L%	/ / ! S%	/ / ! W%

T0II%AJKN"L%	/ / ! S%	/ / ! W%

* + , (- .

Table 15. Boot Device Selection

! 5 + %<"I"P1FGH%	TGG1%4G["%	T5 5 ;`<>=%	9 685`W,%	9 685`WY%

&'$ " + + 4%4GH1LGII"L%

&&$

&($: FV3Z<Q"" [%@* ! ; %

&S$ 6"LFQ3"L0I2%

%

&S$($&$ R"01JL"2

&S$($($ @* ! ; %TIGPU%>\1"LH0I%6FH% / "2PLFQ1FGH%

Table 20. UART Block External Pin Description

6FH%A0K"%	;MQ"%	/ "2PLFQ1FGH%

&SS&$ R"01JL"2%

&SW($ 8 ! % ! a%TIGPU%>\1"LH0I%6FH% / "2PLFQ1FGH%

Table 22. IR RX Block External Pin Description

6FH%A0K"%	;MQ"%	/ "2PLFQ1FGH%

&S$,$&$ R"01JL"2%

&S$,$($ <K0L1%40L[%4GH1LGII"L%>\1"LH0I%6FH%/"2PLFQ1FGH%

Table 24. Smart Card Controller External Pin Description

6FH%A0K"%	;MQ"%	/"2PLFQ1FGH%

& . $: / + 8 % ; L0H2KF11"L%

Table 27. HDMI Block External Pin Description

6FH%A0K"%	8) 5 %	/ "2PLFQ1FGH%

&X$ * J [FGZ8H%8H1"L0OP"%

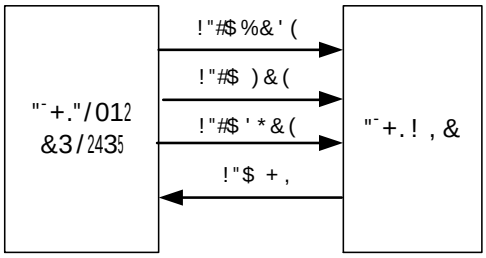


Figure 6. I2S Audio-In Master Mode Interface Configuration

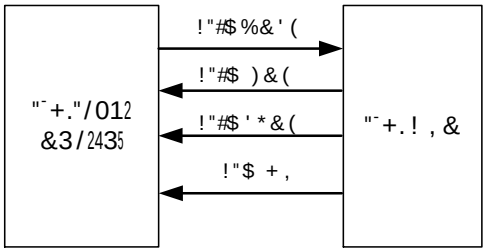


Figure 7. I2S Audio-In Slave Mode Interface Configuration

Table 28. Audio-In Block External Pin Description

6FH%A0K"%	;MQ"%	/ "2PLFQ1FGH%

&-$ * J [FGZ 5 J1%8H1"L0OP"%

* + , (- .

&,$ 648%>\QL"22%($'%

Table 30. PCI Express 2.0 Block External Pin Description

6FH%A0K"%	85%<10H[0L[%	;MQ"%	/ "2PLFQ1FGH%

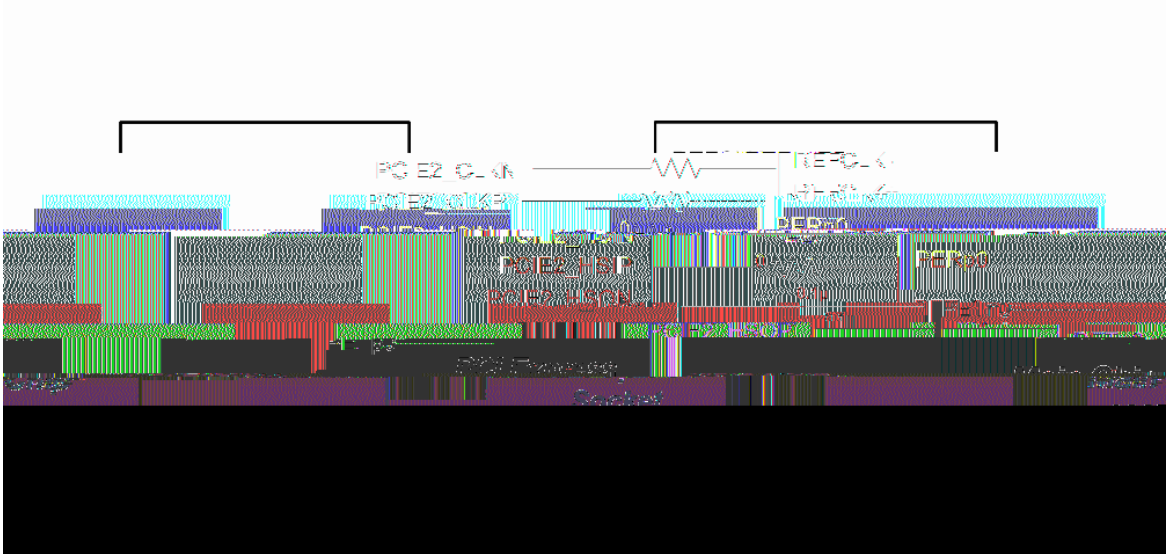


Figure 10. Typical PCI Express 2.0 Application

&Y$ >13"LH"1%4GH1LGII"L%

Table 31. Ethernet 10/100/1000M Block External Pin Description

6FH%A0K"%	;MQ"%	

Figure 11. Relationship of PCIe and Ethernet Block

Figure 12. Typical Gigabit Ethernet Application

* + , (- .%

(&$; L0H2QGL1% + G [JI"%

(($ 40L[%!"0["L%4GH1LGII"L%

Table 34. Card Reader Block External Pin Description

6FH%A0K"%	;MQ"%	/ "2PLFQ1FGH%

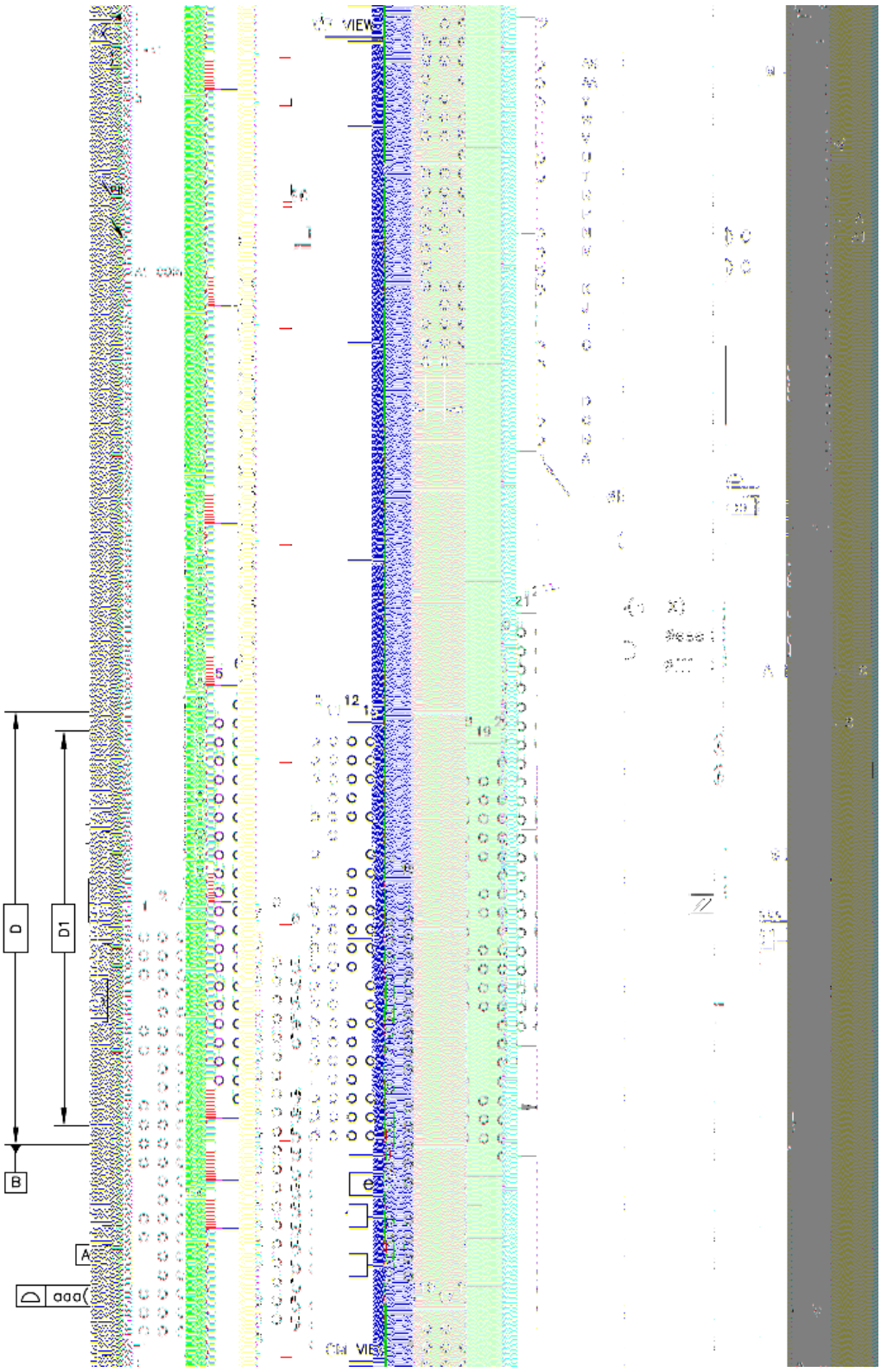
(S$ < / 8 5 %

(W$ <GI["LFHV% ! "0IG] %6LG0FI"%

Table 36. Classification Reflow Profile

6LG0FI"%R"01JL"%	6NZRL""%*22"KNIM%

(. $ + "P3OHFPOI% / FK"H2FGH2%



(X$ 5L["LFHV%8H0GLK01FGH%

Table 37. Ordering Information